REMARKS

STATUS OF CLAIMS

Claims 1-18, 20-22, 24-28 and 31 were previously and are currently pending and under consideration.

Claims 20-22 and 24-28 are allowed.

Claims 1-5, 7-16, 18 and 31 are rejected.

Claim 6 is objected to as being allowable if amended into independent form.

Claims 7-12 and 31 are cancelled herein without disclaimer or prejudice.

Claims 1, 2, 5 and 13-18 are amended herein.

Therefore, claims 1-6, 13-18, 20-22 and 24-28 remain pending for reconsideration, which is respectfully requested.

No new matter is being presented, and approval and entry are respectfully requested.

REJECTIONS UNDER 35 USC §102 and §103

Claims 1-5 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hartnett (US Patent No. 6,167,479) in view of Kim (US Patent No. 6,343,353). Kim is newly cited, and, thus, newly relied upon. This rejection is traversed and reconsideration is requested.

Claims 7, 8, 10-12, 14, 15, and 16 are rejected under 35 U.S.C. §102(e) as anticipated by Hartnett.

Claims 9, 13 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hartnett in view of Swoboda (US Patent No. 6,553,513).

Claim 31 is rejected under 35 USC 102(e) as being anticipated by Hartnett (US Patent No. 6,167,479).

Rejected pending independent claims are 1, 7, 11 and 31. Independent claims 7 (including dependent claim 8-10 thereof) and 31 are cancelled without disclaimer or prejudice.

Claim 6 is objected to as being allowable if amended into independent form.

It is believed that dependent claim 17 is also objected to as being allowable if rewritten

into independent form, because of box 7 in Office Action Summary and the Office Action does not provide a rejection rationale to reject dependent claim 17). Independent claim 11 and dependent claim 12 thereof are cancelled without disclaimer or prejudice and dependent claim 17, which depends from cancelled independent claim 11 and cancelled dependent claim 12, is rewritten into independent form. Therefore, it is understood that new independent claim 17, including dependent claims 13-16 and 18 thereof, are allowable.

Dependent claim 2 is amended for clarity, and support for the claim amendment can be found, for example, in page 18, lines 17-25 of the present Application.

Therefore, the rejection of independent claim 1 is hereby traversed and patentability of new independent claim 17 is discussed, as follows:

Independent claim 1 is amended by providing, "a rewritable register ***prescribing a number of cycles*** from ***when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue an immediately subsequent instruction that is the same ~~instructions~~ as the instruction of said specific application-purpose instruction operation unit***, wherein the instruction of said specific application-purpose instruction occupies an operating unit source." Dependent claim 5 is amended to be consistent with amended independent claim 1. Support for the claim amendments can be found, for example, on page 39, line 23 to page 40, line 23 of the present Application.

Accordingly, the claimed present invention's "rewritable register" provides a benefit of alteration of the function of instruction without depending on instruction of an intellectual property (IP) and without changing the core control unit to solve a problem of a resource conflict and register conflict. This is done only by setting parameters relating to the latency of instruction issue control of the CPU (e.g., claim 1). In contrast to Hartnett and Kim, the claimed present invention as recited in amended independent claim 1 provides:

> 1. (CURRENTLY AMENDED) A processing apparatus, comprising:
>
> a control unit processing an operation instruction, which does not have a functional specification, as a specific application-purpose operation instruction;
>
> a specific application-purpose instruction operating unit supporting a flexible pipeline structure and carrying out an operation of the specific application-purpose operation instruction

for each application field; and

a rewritable register prescribing a number of cycles ***from when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue an immediately subsequent instruction that is the same ~~instructions~~ as the instruction of said specific application-purpose instruction operation unit***, wherein the instruction of said specific application-purpose instruction occupies an operating unit source.

The present invention includes also an instruction control mechanism for handling exceptions that an ordinary operation instruction has (e.g., claim 17).

Therefore, a basic benefit of the claimed present invention as recited in the claims, such as for example independent claims 1 and 17, is that the freedom of instruction system accompanying IP development can be increased without changing the core control circuit and man-hour of validation logics can be decreased, so that development of instruction sets is made possible as efficiently as in the case of ASIC.

More particularly, in contrast to Kim and Hartnett, as recited in independent claims 1 and 17, a control of exceptions in the present invention is performed by a mechanism that creates an interruption operation for exceptions of operations including calculations that cannot be handled by ordinary operating units. According to the present invention, any type of IP including a mechanism that can incorporate an exception handler, such as a zero-division in a division process as an ordinary soft routine, can be implemented without changes to the controller of the CPU.

As a benefit, with regard to the resource conflict, when IP supports a pipeline structure, the present invention can realize a control mechanism that can issue instructions independently of outputs or results without changing the configuration of the CPU controller and through circuitry similar to that used in the control of issuing ordinary operation instructions. The IP-dependent instructions can be optimized by replacing the "user-defined instructions" by instruction functions dependent on the implemented IP and setting parameters of latency as expansion of functions to compliers, assemblers, and instruction-level simulators. In short, user-defined instructions that do not depend on the specific application-purpose instructions as a instruction set can be handled in the same manner as the case of ordinary instructions by implementing an IP. The IP can be implemented without changing the control issue circuitry of the CPU. This enables ASIC development of the CPU as an implementing method that supports

reconfigurable instructions. The ASIC development of the CPU according to the present invention is quite different from an ordinary ASIC.

The present Application at page 38, line 23 to page 40, line 23 describes the above-mentioned reconfiguration of control method.

Kim, which is relied upon by the Office Action in page 3 to meet the claimed present invention's "rewritable register prescribing a number of cycles," is directed to micro-controller access to an external memory according to the characteristics of the external memory (Abstract, column 2, lines 23-53). In particular, Kim discusses an MCU capable of accessing an external memory having a different access time using a microcode (column 3, lines 11-19) and discusses a WAIT register for cycle extension data (columns 3 and 4). However, Kim's cycle extension relates to accessing external memory, and Kim fails to disclose or suggest and differs from the claimed present invention's, "a rewritable register ***prescribing a number of cycles*** from ***when an instruction of said specific application-purpose instruction operating unit is issued to when it becomes possible to issue an immediately subsequent instruction that is the same ~~instructions~~ as the instruction of said specific application-purpose instruction operation unit***, wherein the instruction of said specific application-purpose instruction occupies an operating unit source" (e.g., amended independent claim 1).

Also in contrast to Kim and Hartnett, the claimed present invention as recited in independent claim 17 provides:

> 17. (CURRENTLY AMENDED) ~~The~~An exception processing method ~~according to claim 12, further comprising:~~ of a specific application-purpose operation instruction detecting an operation exception which occurs during execution of a specific application-purpose operation instruction and carrying out an exceptional processing when the operation exception is detected, the exception processing method comprising:
>
> saving a context after an execution of a program has been interrupted;
>
> ***storing a value in a register or a flag indicating that an instruction address***, which has interrupted the execution of a program, ***is to detect the operation exception that occurs during the execution of the specific application-purpose operation ~~instruction, and~~instruction***;
>
> ***confirming whether the operation state has been set to a state indicating ~~whether~~ detection of the operation exception, which occurs during the execution of a specific***

***application-purpose operation instruction*~~*is detected or not,*~~
by referring to the content of said register or said flag;

carrying out the exceptional processing when confirmed according to the confirming that the operation exception has been detected during the execution of the specific application-purpose operation instruction; and

returning from an interruption.

In view of the claim amendments and remarks, withdrawal of the rejection of pending claims and allowance of pending claims is respectfully requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

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